

IN THE CLAIMS

- 1 1. (currently amended) A process for fabricating an electronic device, the process
2 comprising:
 - 3 (a.) forming a first dopant blocking layer at a first temperature; and
 - 4 (b.) forming a second dopant blocking layer at a second temperature over said first
5 dopant blocking layer,
 - 6 said first and second dopant blocking layers being disposed between a semi-insulating
7 layer and a p-type layer.
- 1 2. (original) A process as recited in claim 1, wherein said first temperature is lower than
2 said second temperature.
- 1 3. (original) A process as recited in claim 1, wherein the process further comprises:
2 forming a third dopant blocking layer between said first and said second dopant
3 blocking layers.
- 1 4. (original) A process as recited in claim 1, wherein said first dopant blocking layer is
2 formed over a vertical sidewall of a mesa and over a horizontal surface of a substrate; and
3 said first dopant blocking layer has a substantially uniform thickness.
- 1 5. (original) A process as recited in claim 1, wherein said first and said second blocking
2 layers are InAlAs.
- 1 6. (original) A process as recited in claim 3, wherein said third dopant blocking layer is
2 chosen from the group consisting essentially of InP, InGaP, InGaAs, or InGaAsP .
- 1 7. (original) A process as recited in claim 1, wherein said first temperature lies in the
2 range of approximately 500°C to approximately 570°C.
- 1 8. (original) A process as recited in claim 4, wherein said thickness is in the range of
2 approximately 50 nm to approximately 100 nm.

- 1 9. (original) A process as recited in claim 1, wherein said second dopant blocking layer
2 has a vertical portion and said vertical portion has a thickness in the range of
3 approximately 30 nm to approximately 100 nm.
- 1 10. (original) A process as recited in claim 1, wherein said first and second dopant
2 blocking layers are InGaAlAs.
- 1 11. (original) A process as recited in claim 1, wherein said first dopant blocking layer is
2 disposed above a p-type layer and said second dopant blocking layer is disposed below a
3 semi-insulating layer.
- 1 12. (original) A process as recited in claim 1, wherein said first dopant blocking layer is
2 disposed below a p-type layer and said second dopant blocking layer is disposed above a
3 semi-insulating layer.
- 1 13. (original) A process for fabricating an optoelectronic device as recited in claim 1,
2 wherein said second temperature lies in the range of approximately 600° C to
3 approximately 650° C.
- 1 14. (previously amended) A process as recited in claim 1, wherein said first and said
2 second dopant blocking layers are formed by MOVPE.
- 1 15. (previously amended) A process as recited in claim 1, wherein said first and said
2 second dopant blocking layers are formed by MBE.
- 1 16. (original) A process as recited in claim 15, wherein said first temperature lies in the
2 range of approximately 400° C to approximately 470° C.
- 1 17. (original) A process as recited in claim 15, wherein said second temperature lies in
2 the range of approximately 500° C to approximately 550° C.
- 1 18. (original) A process as recited in claim 14, wherein said first temperature is in the
2 range of approximately 500° C to approximately 570° C.
- 1 19. (original) A process as recited in claim 14, wherein said second temperature lies in
2 the range of approximately 600 ° C to approximately 650 ° C.
- 1 20. (currently amended) A process for fabricating an electronic device, the process
2 comprising:

- 3 (a.) forming a first InAlAs layer at a first temperature; and
 - 4 (b.) forming a second InAlAs layer at a second temperature over said first InAlAs
 - 5 layer,
 - 6 said first and second InAlAs layers being disposed between a semi-insulating layer and a
 - 7 p-type layer .
- 1 21. (original) A process as recited in claim 20, wherein said first temperature is lower
 - 2 than said second temperature.
- 1 22. (original) A process as recited in claim 20, wherein the process further 2 comprises:
 - 2 forming a layer of undoped InP between said first and said second InAlAs layers.
- 1 23. (original) A process as recited in claim 20, wherein said first InAlAs layer is formed
 - 2 over a vertical sidewall of a mesa and over a horizontal surface of a substrate; and
 - 3 wherein said first InAlAs layer has a substantially uniform thickness.
- 1 24. (original) A process as recited in claim 20, wherein said first InAlAs layer is disposed
 - 2 above a p-type layer and said second InAlAs layer is disposed below a semi-insulating
 - 3 layer.
- 1 25. (original) A process a recited in claim 20, wherein said first InAlAs layer is disposed
 - 2 below a p-type layer and said second InAlAs layer is disposed above a semi-insulating
 - 3 layer.
- 1 26. (original) A process for fabricating an electronic device as recited in claim 20,
 - 2 wherein said second temperature lies in the range of approximately 600°C to
 - 3 approximately 650 °C.
- 1 27. (original) A process as recited in claim 20, wherein said first temperature lies in the
 - 2 range of approximately 500 °C to approximately 570 °C.
- 1 28. (original) A process as recited in claim 20, wherein said first and said second dopant
 - 2 blocking layers are formed by MOVPE.
- 1 29. (original) A process as recited in claim 20, wherein said first temperature lies in the
 - 2 range of approximately 400 °C to approximately 470 °C.

1 30. (original) A process as recited in claim 20, wherein said second temperature lies in
2 the range of approximately 500° C to approximately 550° C.

1 31. (original) A process as recited in claim 20 wherein said first and said second dopant
2 blocking layers are formed by MBE.

Claims 32-58 (withdrawn)

59 (cancelled)

1 60. (currently amended) A process as recited in claim 1 wherein the p-type layer includes
2 a Zn dopant, and the semi-insulating layer includes an Fe dopant.

61 (cancelled)

1 62. (currently amended) A process as recited in claim 20 wherein the p-type layer
2 includes a Zn dopant, and the semi-insulating layer includes an Fe dopant.